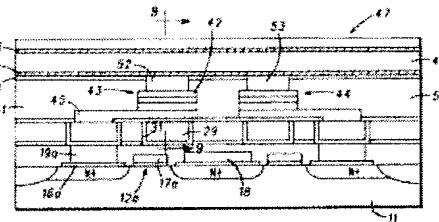


Magnetic random access memory and fabricating method thereof**Publication number:** TW466486 (B)**Publication date:** 2001-12-01**Inventor(s):** DURLAM MARK [US]; KERSZYKOWSKI GLORIA [US]; SLAUGHTER JON [US]; ZHU THEODORE [US]; CHEN EUGENE [CN]**Applicant(s):** MOTOROLA INC [US]**Classification:****- International:** G11C11/15; H01L21/8246; H01L27/22; G11C11/02; H01L21/70; H01L27/22; (IPC1-7): G11C11/14**- European:** G11C11/15; H01L21/8246M; H01L27/22; Y01N4/00**Application number:** TW19990114830 20000128**Priority number(s):** US19980144686 19980831**Also published as:** US6174737 (B1) US5940319 (A)**Abstract of TW 466486 (B)**

An improved and novel MRAM device with magnetic memory elements and circuitry for controlling magnetic memory elements is provided. The circuitry, for example, transistor (12a) having a gate (17a), a drain (18) and a source (16a) is integrated on a substrate (11) and coupled to a magnetic memory element (43) on the circuitry through a plug conductor (19a) and a conductor line (45). The circuitry is fabricated first under the CMOS process and then magnetic memory elements (43, 44). Digit line (29) and bit line (48) are placed under and on top of magnetic memory element (43), respectively, and enabled to access magnetic memory element (43). These lines are enclosed by a high permeability layer (31, 56, 58) excluding a surface facing magnetic memory element (43), which shields and focuses a magnetic field toward magnetic memory element (43).



Data supplied from the esp@cenet database — Worldwide